



## Results from the 141 Respondents to the ESL Now! Online Survey

[Note: Percentages may not total 100 due to rounding]

July 2005

### 1) Which best describes your background?

- 1** Hardware engineer **29.8%**
- 2** Software engineer **5.7%**
- 3** Hardware verification engineer **10.6%**
- 4** Software verification engineer **0.7%**
- 5** IP developer **2.1%**
- 6** CAD team member **12.1%**
- 7** Physical designer **0.7%**
- 8** Systems engineer/architect **17.7%**
- 9** Engineering management **10.6%**
- 10** Non-engineering management **2.1%**
- 11** Other **7.8%** (please specify)
  - Customer consultant
  - EDA & IP distributor
  - Sales
  - TME
  - Press
  - Hardware & CAD Engineer
  - R&D
  - Researcher (2)
  - Research/Education

### 2. What applications are you involved in? (Check all that apply)

- 1** Wireless **16.7%**
- 2** Automotive **4.2%**
- 3** Computing **13.0%**
- 4** Consumer **9.6%**
- 5** Multimedia **13.6%**
- 6** Defense and Aerospace **6.5%**
- 7** Imaging and DSP **12.2%**
- 8** Communication **19.3%**
- 11** Other: **4.8%** (please specify)
  - Power
  - All silicon IP
  - Industry
  - Storage
  - ASIC Design
  - ATE
  - Design Automation
  - Hardware/Software coverification
  - EDA (2)
  - EDA Tools (2)

**3. What type of designs you are currently working on? (Check all that apply)**

- <sub>1</sub> ASIC **24.7%**
- <sub>2</sub> SoC **31.7%**
- <sub>3</sub> Full-custom (>50% of chip) **6.6%**
- <sub>4</sub> ASSP **4.4%**
- <sub>5</sub> FPGA **27.7%**
- <sub>6</sub> Other **4.8%** (please specify):
  - Co-Design
  - EDA
  - EDA Software for ASICs and SOCs
  - Embedded tools design
  - Manual circuit design
  - SystemC-based design
  - Target H/W not yet defined
  - Tools Development

**4. What aspects of this design are you addressing? (Check all that apply)**

- <sub>1</sub> System specification **15.0%**
- <sub>2</sub> Architectural modeling **16.1%**
- <sub>3</sub> System-level virtual prototyping **11.5%**
- <sub>4</sub> RTL design **16.3%**
- <sub>5</sub> Functional verification **16.1%**
- <sub>6</sub> Firmware development **3.9%**
- <sub>7</sub> Application software development **5.9%**
- <sub>8</sub> Embedded software tools development **5.9%**
- <sub>9</sub> Physical design/synthesis **8.7%**
- <sub>10</sub> Other (please specify): **0.9%**
  - Circuit design
  - Software in EDA
  - SystemC hardware design

**5. What languages do you use/plan to use for the design aspects?**

Check <input checked="" type="checkbox"/> all that apply	Current Design	Next Design
C or C++	23.1% <input type="checkbox"/> <sub>1</sub>	16.3% <input type="checkbox"/> <sub>1</sub>
MATLAB	8.0% <input type="checkbox"/> <sub>2</sub>	8.3% <input type="checkbox"/> <sub>2</sub>
SystemC	13.4% <input type="checkbox"/> <sub>3</sub>	22.8% <input type="checkbox"/> <sub>3</sub>
SystemVerilog	2.7% <input type="checkbox"/> <sub>4</sub>	9.9% <input type="checkbox"/> <sub>4</sub>
UML	3.0% <input type="checkbox"/> <sub>5</sub>	5.8% <input type="checkbox"/> <sub>5</sub>
Verilog	28.1% <input type="checkbox"/> <sub>6</sub>	21.4% <input type="checkbox"/> <sub>6</sub>
VHDL	20.1% <input type="checkbox"/> <sub>7</sub>	13.8% <input type="checkbox"/> <sub>7</sub>
Other (please specify]	1.7% <input type="checkbox"/> <sub>8</sub>	1.8% <input type="checkbox"/> <sub>8</sub>

“Other – Current”

- MaxSimC
- Module compiler
- Assembly, Java
- Simulink
- Mobius

“Other – Next”

- Assembly, Java
- MaxSimC
- Mathcad
- Simulink
- Mobius

## 6. What languages do you use/plan to use for the verification aspects?

Check <input checked="" type="checkbox"/> all that apply	Current Design	Next Design
C or C++	22.6% <input type="checkbox"/> <sub>1</sub>	17.7% <input type="checkbox"/> <sub>1</sub>
e	7.5% <input type="checkbox"/> <sub>2</sub>	8.1% <input type="checkbox"/> <sub>2</sub>
MATLAB	7.2% <input type="checkbox"/> <sub>3</sub>	6.6% <input type="checkbox"/> <sub>3</sub>
OpenVera	2.4% <input type="checkbox"/> <sub>4</sub>	2.6% <input type="checkbox"/> <sub>4</sub>
SystemC	14.7% <input type="checkbox"/> <sub>5</sub>	24.4% <input type="checkbox"/> <sub>5</sub>
SystemVerilog	3.4% <input type="checkbox"/> <sub>6</sub>	8.9% <input type="checkbox"/> <sub>6</sub>
UML	1.0% <input type="checkbox"/> <sub>7</sub>	1.1% <input type="checkbox"/> <sub>7</sub>
Verilog	22.3% <input type="checkbox"/> <sub>8</sub>	16.2% <input type="checkbox"/> <sub>8</sub>
VHDL	16.4% <input type="checkbox"/> <sub>9</sub>	13.3% <input type="checkbox"/> <sub>9</sub>
Other (please specify)	2.4% <input type="checkbox"/> <sub>10</sub>	1.1% <input type="checkbox"/> <sub>10</sub>

"Other – Current"

- PSL (3)
- Mathcad
- Mobius
- Internal solution
- LISA

"Other – Next"

- PSL (2)
- Mathcad
- Mobius

## 7. How much of your next design will be created from the reuse of existing IP?

- <sub>1</sub> 0 – 25% **20.6%**
- <sub>2</sub> 25 – 50% **40.4%**
- <sub>3</sub> 50 -75% **29.8%**
- <sub>4</sub> 75 – 100% **9.2%**

## 8. ESL methodologies can significantly improve productivity.

- <sub>1</sub> Strongly Agree **45.4%**
- <sub>2</sub> Agree **53.2%**
- <sub>3</sub> Disagree **0.7%**
- <sub>4</sub> Strongly Disagree **0.7%**

## 9. Who is driving ESL in your company?

- <sub>1</sub> Senior management **17.0%**
- <sub>2</sub> Engineering management **21.3%**
- <sub>3</sub> Non-engineering management **0.7%**
- <sub>4</sub> Hardware engineering **10.6%**
- <sub>5</sub> Software engineering **0.7%**
- <sub>6</sub> Verification engineering **9.2%**
- <sub>7</sub> System engineer/architect **15.6%**
- <sub>8</sub> Others.....**5.7%**
- <sub>9</sub> No one! **19.1%**

## 10. Is there anything missing from ESL? Please explain.

- There is one thing that is really missing from this website: A detailed explanation of what is ESL! Path to implementation just starting, missing equivalency checking, ability to specify/analyze quantities for delay, power, etc.
- UML or other higher level languages are tools not yet a complete methodology. In the semiconductor discipline, the biggest hardware problem today is the functional verification of RTL. No ESL methodology today ties the architecture, design and verification.
- SystemC synthesis capabilities comparable to those of VHDL/Verilog.
- Very important to us is 1<sup>st</sup>: reuse of the testbench and 2<sup>nd</sup>: use ESL model for top-down design.
- No one is demonstrating quality of results compared to best hand-designs.
- ESL includes modeling and simulation of architecture and function of the chip PLUS the system in which the chip is to be used. 60% of design errors are in specifications. This can only be overcome by making specifications executable. There are now some companies addressing the seamless design flow from ESL to RTL either by behavioral synthesis or by equivalence checking. However, the maturity of their technology is not good enough to address all problems in a real engineering life.
- Common methodology and usage model from different EDA vendors.
- A direct path from algorithm to netlist.
- A workable methodology to develop a truly executable specification based upon formal mathematical techniques. An adaptive feedback algorithm to ensure verification of the changes that affect the system specification.
- ESL = English as a Second Language. I have no desire to learn what else it might mean.
- No
- A new system design methodology.
- MATLAB is best for DSP
- Users
- Plug-and-Play IP library.
- Come and listen to ESL panel at DAC: Tales from the trenches
- Perhaps an online forum/chat or vbulletin-like interface will be beneficial..Thank you!
- Ease of integration with other tools, transparency, support for “manual” tweaking, tools are still very complex.
- A viable agreement on definition. The kitchen sink is already there. I expect it will do the dishes and put out the cat, too.
- The Maxfield report missed out an important, IMHO, point of view, which is the application view. Though some people would say algorithm is application, I would say the conceptual originality is different. Algorithms for EE persons are things like MPEG4.
- Something like tool.
- Standardization and tool support.
- What a strange question. Of course there is. The complete flow and methodology is incomplete, ill defined and for many companies the purpose of it is unclear. ESL Now needs to do a lot more work in the area of public education.
- Simulation speed is a concern.
- A coherent definition.
- Better design tools, not necessarily the C->RTL option.